UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/614,523 | 07/03/2003 | Simeon Furrer | CH920000067US1 | 7648 |

48813 7590 09/04/2008

LAW OFFICE OF IDO TUCHMAN (YOR)
ECM #72212
PO Box 4668
New York, NY 10163-4668

| EXAMINER | |
|---|---|
| WILLIAMS, LAWRENCE B | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2611 | |

| NOTIFICATION DATE | DELIVERY MODE |
|---|---|
| 09/04/2008 | ELECTRONIC |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

pair@tuchmanlaw.com
idotuchman@gmail.com

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/614,523 | FURRER ET AL. | |
| | Examiner | Art Unit | |
| | LAWRENCE B. WILLIAMS | 2611 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *22 November 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-22 and 28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22, 28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 19-20, 28 are rejected under 35 U.S.C. 102(e) as being anticipated by Lewin et al. (US Patent 6,587,476 B1).

(1) Regarding claim 1, Lewin et al. discloses in Fig(s). 5, 6, a communication device (14) for processing outgoing and incoming packets, the device comprising: a plurality of signal processing units (Fig. 5, elements 82, 84) connected in sequence (col. 12, lines 29-42), each signal processing unit being clocked by a common clock signal (Fig. 6, Lewin et al. discloses TxCLK being supplied to Ethernet, HDLC, and VDSL transceivers. Fig. 6, shows a similar configuration for RxCLK); a mode line connected to each signal processing unit for switching each signal processing unit between a transmit mode and a receive mode (Fig. 6 discloses TxEnable/RxEnable, to/from Ethernet/HDLC Converter, 100. The HDLC would have to be operating in a Normal Response mode (used most frequently in multi-port lines; only transmit/receive when and only when it is instructed to do so) for proper operation of the system and thus would also have a mode line (not shown) for operation, since Asynchronous Response

Mode and Asynchronous Balanced Mode (not widely used) of the HDLC would require a second HDLC); and a control line (Fig. 5, 6; col. 11, lines 50-53) to which each signal processing unit is connected, the control line communicating flow control information either in the transmit mode to at least one of the preceding signal processing units or in the receive mode to at least one of the following signal processing units. As disclosed in col. 11, lines 50-53, the controller (90) functions to control the operation of the transceivers 82, 84, 86. Control flow information to at least one of the preceding transceivers in a transmit mode and control flow information to at least one of the following in a receive mode would be an inherent feature, since Lewin et al. discloses the invention operating bi-directional (see bi-directional arrows), i.e., a transmit and receive mode of operation.

(2) Regarding claim 19, Lewin et al. also discloses the device according to claim 1, wherein each signal processing unit is usable for the transmit and receive mode. Lewin et al. discloses in Fig. 5, the signal processing units 82, 84, and 86 as transceivers.

(3) Regarding claim 20, Lewin et al. discloses in Fig(s). 5, 6, a transceiver unit adapted to communicate with a buffer unit (108) via a bus system (arrow shows connectivity via bus), the transceiver comprising a transceiver controller (Fig. 6, element 110) and a communication device communication device (Fig. 5, element 14, Fig. 6, element 100), both transceiver controller and communication device being interconnected (arrows show interconnectivity), said communication device comprises: a plurality of signal processing units (Fig. 5, elements 82, 84) connected in sequence (col. 12, lines 29-42), each signal processing unit being clocked by a common clock signal (Fig. 6, Lewin et al. discloses TxCLK being supplied to Ethernet, HDLC, and VDSL transceivers. Fig. 6, shows a similar configuration for RxCLK); a mode line

connected to each signal processing unit for switching each signal processing unit between a transmit mode and a receive mode (Fig. 6 discloses TxEnable/RxEnable, to/from Ethernet/HDLC Converter, 100. The HDLC would have to be operating in a Normal Response mode (used most frequently in multi-port lines; only transmit/receive when and only when it is instructed to do so) for proper operation of the system and thus would also have a mode line (not shown) for operation, since Asynchronous Response Mode and Asynchronous Balanced Mode (not widely used) of the HDLC would require a second HDLC); and a control line (Fig. 5, 6; col. 11, lines 50-53) to which each signal processing unit is connected, the control line communicating flow control information either in the transmit mode to at least one of the preceding signal processing units or in the receive mode to at least one of the following signal processing units. As disclosed in col. 11, lines 50-53, the controller (90) functions to control the operation of the transceivers 82, 84, 86. Control flow information to at least one of the preceding transceivers in a transmit mode and control flow information to at least one of the following in a receive mode would be an inherent feature, since Lewin et al. discloses the invention operating bi-directional (see bi-directional arrows), i.e., a transmit and receive mode of operation.

(4) Regarding claim 28, Lewin et al. discloses in Fig(s). 5, 6, a baseband system (Lewin et al. discloses Ethernet and VDSL transceivers, which are well-known to one of ordinary skill in the art to be baseband components) comprising a communication device (14), including a plurality of signal processing units (Fig. 5, elements 82, 84) connected in sequence (col. 12, lines 29-42), each signal processing unit being clocked by a common clock signal (Fig. 6, Lewin et al. discloses TxCLK being supplied to Ethernet, HDLC, and VDSL transceivers. Fig. 6, shows a similar configuration for RxCLK); a mode line connected to each signal processing unit for

switching each signal processing unit between a transmit mode and a receive mode (Fig. 6 discloses TxEnable/RxEnable, to/from Ethernet/HDLC Converter, 100. The HDLC would have to be operating in a Normal Response mode (used most frequently in multi-port lines; only transmit/receive when and only when it is instructed to do so) for proper operation of the system and thus would also have a mode line (not shown) for operation, since Asynchronous Response Mode and Asynchronous Balanced Mode (not widely used) of the HDLC would require a second HDLC); and a control line (Fig(s). 5, 6; col. 11, lines 50-53) to which each signal processing unit is connected, the control line communicating flow control information either in the transmit mode to at least one of the preceding signal processing units or in the receive mode to at least one of the following signal processing units. As disclosed in col. 11, lines 50-53, the controller (90) functions to control the operation of the transceivers 82, 84, 86. Control flow information to at least one of the preceding transceivers in a transmit mode and control flow information to at least one of the following in a receive mode would be an inherent feature, since Lewin et al. discloses the invention operating bi-directional (see bi-directional arrows), i.e., a transmit and receive mode of operation.

3. Claims 2-3, 11-12, 14-15, 17-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Wong et al. (US 2002/0120831 A1).

(1) With regard to claim 2, Wong et al. discloses in Fig. 3, a communication device for processing outgoing packets, the device comprising: a plurality of signal processing units (Stage i, Pipeline 1, Stage i +1, Pipeline 1) connected in sequence, each signal processing unit being clocked by a common clock signal (In Fig. 3, Wong et al. discloses all inputs fed by common clock signal); and a control line (stall) to which each signal processing unit is connected, the

control line communicating flow control information to stall at least one of the signal processing units following in the signal processing chain for feedback control of the signal processing units to at least one of the preceding signal units (col. 1, paragraph 0010; Wong et al. discloses the stalling means arranged such that when a pipeline generates a stall signal at stage i, all stages **up to** and including stage i are stalled. Stalling the stages "up to" would constitute feedback control.)

(2) With regard to claim 3, Wong et al. discloses in Fig. 3, a communication device for an incoming packet, the device comprising: a plurality of signal processing units (Stage i, Pipeline 1, Stage i +1, Pipeline 1) connected in sequence thereby forming a signal processing chain, each signal processing unit being clocked by a common clock signal (In Fig. 3, Wong et al. discloses all inputs fed by common clock signal); and a control line (stall) to which each signal processing unit is connected, the control line communicating flow control information to stall at least one of the signal processing units following in the signal processing chain for feedforward control of the signal processing units to at least one of the preceding signal units (col. 1, paragraph 0010; Wong et al. that if required, some or all of the later stages could be stalled. Stalling the later stages would constitute feedforward control of the stages).

(3) With regard to claim 11, claim 11 inherits all limitations of claim 2, above. As noted above, Wong et al. discloses all limitations of claim 2. Furthermore, Wong et al. also discloses in Fig. 3, wherein each signal processing unit (42, 52) is connected via a logic unit (44, 54) to the control line (stall).

(4) With regard to claim 12, claim 12 inherits all limitations of claim 3, above. As noted above, Wong et al. discloses all limitations of claim 3. Furthermore, Wong et al. also discloses in

Fig. 3, wherein each signal processing unit (42, 52) is connected via a logic unit (44, 54) to the control line (stall).

(5) Regarding claim 14, claim 14 inherits all limitations of claim 11. Furthermore, Wong et al. also discloses Fig. 3, wherein the logic unit (44) comprises an OR gate.

(6) Regarding claim 15, claim 15 inherits all limitations of claim 12. Furthermore, Wong et al. also discloses Fig. 3, wherein the logic unit (44) comprises an OR gate.

(7) With regard to claim 17, claim 17 inherits all limitations of claim 2, above. Furthermore, Wong et al. also discloses wherein flow control information comprises a hold information indicating to the signal processing units receiving the hold information to stop processing (col. 1, paragraph 0006; Wong et al. discloses stalling an execution of an instruction; thereby stopping processing).

(8) With regard to claim 18, claim 18 inherits all limitations of claim 3, above. Furthermore, Wong et al. also discloses wherein flow control information comprises a hold information indicating to the signal processing units receiving the hold information to stop processing (col. 1, paragraph 0006; Wong et al. discloses stalling an execution of an instruction; thereby stopping processing).

## *Claim Rejections - 35 USC § 103*

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lewin et al. (US Patent 6,587,476 B1) as applied to claim 1 above, and further in view of Sambamurthy et al. US Patent 6,108,713).

As noted above, Lewin et al. discloses all limitations of claim 1. Lewin et al. does not however disclose wherein each signal processing unit comprises a multiplexing unit. However, the signal-processing unit comprising a multiplexing unit is a minor detail. Sambamurthy et al. discloses in Fig. 4E, a signal processing unit (206) comprising a multiplexer (261).

It would have been obvious to one skilled in the art at the time of invention to incorporate the teachings of Sambamurthy et al. as a method of permitting the simultaneous transmission of two or more trains of data over a single channel.

6. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wong et al. (US 2002/0120831 A1) as applied to claim 2 above, and further in view of Sambamurthy et al. US Patent 6,108,713).

As noted above, Wong et al. discloses all limitations of claim 2. Wong et al. does not however disclose wherein each signal processing unit comprises a multiplexing unit. However, the signal-processing unit comprising a multiplexing unit is a minor detail. Sambamurthy et al. discloses in Fig. 4E, a signal processing unit (206) comprising a multiplexing unit (261).

It would have been obvious to one skilled in the art at the time of invention to incorporate the teachings of Sambamurthy et al. as a method of permitting the simultaneous transmission of two or more trains of data over a single channel.

7. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wong et al. (US 2002/0120831 A1) as applied to claim 3 above, and further in view of Sambamurthy et al US Patent 6,108,713).

As noted above, Wong et al. (US 2002/0120831 A1). et al. discloses all limitations of claim 3. Wong et al. (US 2002/0120831 A1). et al. does not however disclose wherein each signal processing unit comprises a multiplexing unit. However, the signal-processing unit comprising a multiplexing unit is a minor detail. Sambamurthy et al. discloses in Fig. 4E, a signal processing unit (206) comprising a multiplexing unit (261).

It would have been obvious to one skilled in the art at the time of invention to incorporate the teachings of Sambamurthy et al. as a method of permitting the simultaneous transmission of two or more trains of data over a single channel.

8. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lewin et al. (US Patent 6,587,476 B1) as applied to claim 1 above, and further in view of Koseki et al. (US Patent 4,686,668).

As noted above, Lewin et al. discloses all limitations of claim 1. Lewin et al. does not disclose wherein each signal processing unit comprises a multiplexer at its input and a demultiplexer at its output. However, the signal-processing unit comprising a multiplexer at its input and a demultiplexer at its output is a minor detail. Koseki et al. discloses in Fig. 4a, a signal-processing unit comprising a multiplexer (42) at its input and a demultiplexer (68) at its output. It would have been obvious to one skilled in the art at the time of invention to incorporate

the teachings of Koseki et al. as a method of permitting the simultaneous transmission of two or more trains of data over a single channel.

9. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wong et al. (US 2002/0120831 A1) as applied to claim 2 above, and further in view of Koseki et al. (US Patent 4,686,668).

As noted above, Wong et al. discloses all limitations of claim 2. Wong et al. does not disclose wherein each signal processing unit comprises a multiplexer at its input and a demultiplexer at its output. However, the signal-processing unit comprising a multiplexer at its input and a demultiplexer at its output is a minor detail. Koseki et al. discloses in Fig. 4a, a signal-processing unit comprising a multiplexer (42) at its input and a demultiplexer (68) at its output. It would have been obvious to one skilled in the art at the time of invention to incorporate the teachings of Koseki et al. as a method of permitting the simultaneous transmission and reception of two or more trains of data over a single channel.

10. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wong et al. (US 2002/0120831 A1) as applied to claim 3 above, and further in view of Koseki et al. (US Patent 4,686,668).

As noted above, Wong et al. discloses all limitations of claim 3. Wong et al. does not disclose wherein each signal processing unit comprises a multiplexer at its input and a demultiplexer at its output. However, the signal-processing unit comprising a multiplexer at its input and a demultiplexer at its output is a minor detail. Koseki et al. discloses in Fig. 4a, a

signal-processing unit comprising a multiplexer (42) at its input and a demultiplexer (68) at its output. It would have been obvious to one skilled in the art at the time of invention to incorporate the teachings of Koseki et al. as a method of permitting the simultaneous transmission and reception of two or more trains of data over a single channel.

11. Claims 10, 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lewin et al. (US Patent 6,587,476 B1) as applied to claim 1, above, and further in view of Freiburg et al. US Patent 5,349,647).

As noted above, Lewin et al. discloses all limitations of claim 1. Lewin et al. does not teach wherein each signal processing unit is connected via a logic unit to the control line (256-258).

However, Freiburg et al. teaches in Fig(s). 3A, 3B, signal processing units (252-256) connected to via a logic unit to a control line (col. 14, lines 12-22). It would have been obvious to one skilled in the art at the time of invention to incorporate the teachings of Freiburg such that the direction of each signal processing unit and accordingly data flow can be alternately programmable. Though Freiburg is silent as to the make up of the logic unit, one or ordinary skill in the art would readily recognize that the use intended by Freiburg could readily be implemented using an OR gate or any combination of logic and thus would be a mere design choice of the user.

12. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lewin et al. (US Patent 6,587,476 B1) as applied to claim 1 above, and further in view of Sambamurthy et al. (US Patent 6,108,713).

As noted above, Lewin et al. discloses all limitations of claim 1 above. Lewin et al. does not disclose the device according to claim 1, wherein the flow control information comprises a hold information indicating to the signal processing units receiving the hold information to stop processing.

However, Sambamurthy et al. discloses a device wherein flow control information comprises a hold information indicating to the signal processing units receiving the hold information to stop processing (col. 13, lines 45-51; desired defer period).

It would have been obvious to one skilled in the art at the time of invention to incorporate the teachings of Sambamurthy et al. as a method of managing data flow through the network.

13. Claim 21, 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin (US 2003/0096634 A1) in view of Lee et al. (US Patent 6,650,880 B1) and further in view of Wong et al. (US 2002/0120831).

(1) With regard to claim 21, Lin discloses in Fig. 5, a transceiver unit adapted to communicate with a buffer via a bus system unit (elements 560, 528, also 544, 548) via a bus system (518, 508 and also 516), the transceiver unit comprising: a transceiver controller (504) and a communication device (564, 532), both transceiver controller and communication device being interconnected, said communication device including: a plurality of signal processing units (572, 536; pg. 4, paragraphs [0040]). Lin discloses the elements 536 and 572 comprising signal

processing units, CRC, FLEC and Whitening modules). Lin does not explicitly disclose the arrangement of the modules. However, Lee et al. teaches in Fig. 3B, signal processing modules/units (336, 344, 352) in a Bluetooth receiver connected in sequence, each signal processing unit being clocked by a common clock signal (364; col. 8, lines 18-22); and a control line to which each signal processing unit is connected, the control line communicating flow control information to at least one of the preceding signal processing units (col. 7, line 66-col. 8, line 17).

It would have been obvious to one skilled in the art at the time of invention to incorporate the teachings of Lee et al. as a method of altering the processing of data signals.

Neither Lin nor Lee et al. explictly disclose the control line communicating control flow information to stall at least one of the preceding processing units for feedback control of the signal processing units.

However, Wong et al. discloses in Fig. 3, a control line (stall) communicating information to stall at least one of a preceding processing units for feedback of signal processing units (col. 1, paragraph 0010; Wong et al. discloses the stalling means arranged such that when a pipeline generates a stall signal at stage i, all stages **up to** and including stage i are stalled. Stalling the stages "up to" would constitute feedback control.)

One skilled in the art at the time of invention would have been motivated to incorporate the teachings of stalling sequential devices as a method of containment of propagation of errors through the system.

(2) With regard to claim 22, Lin discloses in Fig. 5, a transceiver unit adapted to communicate with a buffer unit via a bus system (elements 560, 528, also 544,548) via a bus

system (518, 508 and also 516), the transceiver unit comprising: comprising a transceiver controller (504) and a communication device (564, 532), both transceiver controller and communication device being interconnected, said communication device including: a plurality of signal processing units (572, 536; pg. 4, paragraphs [0040]). Lin discloses the elements 536 and 572 comprising signal processing units, CRC, FLEC and Whitening modules) connected in sequence thereby forming a signal processing chain. Lin does not explicitly disclose the arrangement of the modules. However, Lee et al. teaches in Fig. 3B, signal processing modules/units (336, 344, 352) in a Bluetooth receiver connected in sequence thereby forming a signal processing chain, each signal processing unit being clocked by a common clock signal (364; col. 8, lines 18-22); and a control line to which each signal processing unit is connected, the control line communicating flow control information to at least one of the processing units following the signal processing chain (col. 7, line 66-col. 8, line 17).

It would have been obvious to one skilled in the art at the time of invention to incorporate the teachings of Lee et al. as a method of altering the processing of data signals.

Neither Lin nor Lee et al. explictly disclose the control line to which each signal processing unit is connected to, the control line communicating control flow information to stall at least one of the signal processing following the signal processing chain for feedforward control of the signal processing units.

However, Wong et al. discloses in Fig. 3, a control line (stall) communicating information to stall at least one of signal processing unit following a signal processing chain for feedforward control of the signal processing units. (col. 1, paragraph 0010; Wong et al. discloses if required, one or all of the later stages could be also stalled).

One skilled in the art at the time of invention would have been motivated to incorporate the teachings of stalling sequential devices as a method of containment of propagation of errors through the system.

***Conclusion***

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a.) Fleck et al. discloses in US Patent 6,085,315 Data Processing Device With Loop Pipeline.

b.) Siemers discloses in US Patent 6,061,367 Processor With Pipelining Structure And Method For High-Speed Calculation With Pipelining Processors.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lawrence B Williams whose telephone number is 571-272-3037. The examiner can normally be reached on Monday-Friday (8:00-6:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ghayour Mohammad can be reached on 571-272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lawrence B. Williams

lbw
September 3, 2008

/Lawrence B Williams/
Primary Examiner, Art Unit 2611